Electronic Version

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Description

Method of Forming Silicon-On-Insulator Wafers Having Process Resistant Applications

BACKGROUND OF INVENTION

[0001] The invention relates to semiconductor manufacturing processes, and more particularly to a method of making a silicon-on-insulator wafer.

[0002] In fabricating integrated circuits in conventional bulk semiconductor wafers, wells of either P-type or N-type conductivity are implanted in a substrate of the opposite conductivity. However, in complementary metal oxide semiconductor (CMOS) technology, both p-type and n-type wells are utilized. Source/drain regions are formed by implanting diffusion regions of the opposite n-type or p-type conductivity as the wells to form metal-oxide-semiconductor field effect transistors (MOSFETs). In such integrated circuits, each transistor and/or other device must be electrically isolated from the others in order to work properly. Unfortunately, a relatively large amount of surface area is needed for the electrical isolation of the various transistors, which is in direct opposition with the current needs and goals of size reduction of these devices.

[0003] Another problem with current methods of providing electrical isolation is

junction capacitance between source/drain regions and the bulk substrate. Such junction capacitance tends to increase power consumption and requires higher threshold voltages, which in turn affects the speed at which devices operate, and degrades frequency response.

[0004] In order to deal with the above-mentioned problems, silicon-on-technology (SOI) has been gaining popularity. SOI substrates have a structure in which an active device layer of single crystal silicon is formed over an insulating layer of the substrate. The insulating layer acts to eliminate capacitance between devices formed in the active device layer and the lower bulk layer of the substrate, and prevent the development of electrical paths through the substrate, which can ultimately degrade or destroy surface devices. Use of SOI substrates tends to decrease parasitic capacitance, leading to improvements in speed, reduced power consumption, better frequency response, and resistance to soft errors, while helping to address manufacturability concerns.

[0005] A number of methods are used in producing SOI substrates, the two more popular methods being bonding methods, and separation by ion implanted oxide (SIMOX). In bonding methods, a single crystal silicon wafer is bonded to another single crystal silicon wafer, the surface of which has been thermally oxidized, and then one of the silicon layers is converted to a uniform thin film by mechanical polishing or chemical etching. Bonding methods, however, can be costly and time-

consuming, since two wafers are needed to produce one usable SOI wafer, and time-consuming polishing is required.

[0006] SIMOX is a preferred way of making SOI wafers, as it tends to be less costly than bonding methods. In a SIMOX process, accelerated high-energy oxygen ions are implanted into a single crystal silicon wafer or substrate. The oxygen ions come to rest at selected depths within the substrate in a Gaussian distribution pattern. The result is the formation of a region of implanted oxygen between an upper device layer and a lower bulk layer of the single crystal silicon substrate. The substrate is then annealed to react the implanted oxygen ions with the silicon to form a continuous buried oxide (BOX) layer of silicon dioxide below the upper device layer of the substrate, providing electrical isolation between the upper device layer and the bulk layer of the substrate.

[0007] Unfortunately, two problems are associated with SIMOX processes, which affect the dielectric strength of the BOX and its long-term reliability, as measured by its breakdown voltage. A first problem is the incomplete oxidation of the BOX layer that can occur in some SIMOX processes. Unoxidized regions of silicon atoms (Si) and incompletely oxidized silicon atoms (SiO_x) may remain within the silicon dioxide (SiO_2) BOX layer after processing. Such regions tend to reduce the dielectric strength of the BOX layer and decrease its long-term reliability.

[0008] A second problem has arisen recently due to industry's current goal of making thinner upper device layers of SOI substrates, such upper

device layers also being referred to as "SOI layers". Thin BOX layers formed in substrates having thin SOI layers are more prone to damage during processing to form active devices in the SOI layer. Such processing can damage a thin BOX layer, making it more susceptible to dielectric breakdown.

[0009] However, making a thicker BOX layer is not desired because of greater costs and time requirements for processing. Nonetheless, when thicker BOX layers are used, certain plasma processes can cause charging of the SOI substrate between the SOI layer and the lower bulk layer, leading to charge breakdown, punching through weakened locations of the BOX, thus affecting device performance and increasing device defects. Figure 1 illustrates the dielectric breakdown voltage of the BOX in relation to its thickness. As shown in Figure 1, the breakdown voltage of the BOX is over 80 volts at full thickness for SIMOX wafers, but drops off rapidly with smaller thicknesses.

SUMMARY OF INVENTION

[0010]

According to an aspect of the invention, a method is provided for making SOI wafers having improved electrical isolation in the BOX layer. The method is used for making separation by ion implanted oxide (SIMOX) substrates. In the method, ions are implanted into the substrate in a base dose implant conducted at a first energy level. In a second implant conducted at a second energy level, ions are implanted while the substrate is held at room temperature. In an alternative embodiment, multiple base dose implants are performed, and a single

RT implant is performed, and implants are performed at a plurality of different energy levels. Energy levels and ion implant doses are preferably reduced after initial implants are performed. Thereafter, annealing is performed to cause redistribution of ions within the substrate.

[0011] Alternatively, according to another aspect of the invention, a single base dose implant and multiple RT implants are performed, each implant being conducted at a different energy level. As before, energy levels and ion doses can be reduced in each subsequent implant. In yet another embodiment, multiple base dose implants and multiple RT implants are performed, each implant being conducted at a different energy level. Again, energy levels and ion doses can be reduced with each successive implant. Thereafter, annealing is performed to cause redistribution of ions within the substrate.

BRIEF DESCRIPTION OF DRAWINGS

[0012] Figure 1 is a graph showing degraded BOX properties;

[0013] Figure 2 is a diagram illustrating a SIMOX implantation process to form an SOI wafer;

[0014] Figure 3 is a flowchart showing an embodiment of the invention.

[0015] Figure 4 is a flowchart showing an embodiment of the invention where multiple base dose implantations are used;

[0016] Figure 5 is a flowchart showing an embodiment of the invention where multiple room temperature implantations are used;

[0017] Figure 6 is a graphical illustration of Si inclusion density, with and without processing according to an embodiment of the invention;

[0018] Figure 7 is a graphical illustration showing surface smoothness of an SOI layer;

[0019] Figure 8 provides a graphical illustration of the BOX breakdown voltage for an improved BOX process; and

[0020] Figure 9 is a graphical illustration showing the BOX breakdown voltage for various thicknesses of the BOX layer.

DETAILED DESCRIPTION

[0021] In Figure 2, a single crystal silicon substrate 200 is shown. A buried region 220 is implanted with oxygen ions 210 using an accelerated high-energy oxygen ion beam. This process is known as the first or base dose implant. For illustrative purposes, the SIMOX process is optimized for a nominal silicon-on- insulator layer 230 thickness of between 550 Ã□b 700 Ã□and a nominal BOX thickness of approximately 1350 Ã□b 1550 Ã□The implant dose is preferably in the range of 1×10^{16} to 4×10^{17} ions/cm^2. The oxygen ion implantation energy is preferably between 40 and 240 KeV. The substrate temperature is kept at about 200°C to 600°C during this base dose implant step.

[0022] A second implantation of oxygen ions is performed subsequent to the first implant step. During this second implant, the temperature of the substrate is maintained at room temperature (between 10Â°C and 25Â°

C), such that the second implantation process is called a room temperature (RT) implant. The RT implant of oxygen may be carried out at a lower dose ranging between $5x10^{14}$ to $1x10^{16}$ ions/cm^2, but at the same energy as the base dose. The RT implant acts to amorphize the silicon layer at the depth determined by the energy level. The amorphized layer helps form a continuous BOX layer 220 and enhances internal thermal oxidation (ITOX) during the high temperature anneal that follows. This leads to a BOX layer 220 which has excellent properties when produced.

[0023] A variety of different ions can be used during this second implant step. For example, at times nitrogen ions can be used to passivate the trapped charge which results from broken silicon and oxygen bonds. Nitrogen reacts with free electrons and broken molecules to form stable bonds. However, since active devices are degraded by the presence of nitrogen, nitrogen is not always a good choice for the second implant.

[0024] An annealing step is then performed to redistribute the oxygen ions within the silicon substrate. Annealing tends to sharpen the demarcation between the buried silicon dioxide layer and the silicon layers, that is initially somewhat spread out because the implanted oxygen ions come to rest at different depths in a Gaussian distribution pattern within the substrate. During annealing, the substrate is held at temperature ranging between 1000 and 1400 degrees Celsius for a period of 6 to 10 hours.

[0025] Several embodiments of the invention incorporate internal oxidation to

improve the dielectric properties of the oxide, not just at the surface, as in conventional SIMOX processes, but throughout the BOX layer, especially in the middle of the BOX layer where such areas are likely to be damaged by subsequent processing.

[0026] An embodiment of the invention is illustrated in Figure 3. Whereas in conventional SIMOX processing, all implants are performed at the same energy, in the embodiments shown in Figures 3 through 5, each implant is performed a different energy level than other implants. The combination of dose and energy levels in each implant, and the offset between each implant are key for performing an improved SIMOX process according to the invention.

[0027] In Figure 3, a SIMOX process is provided to produce a high voltage breakdown BOX. In this embodiment, implant energy is offset between the base dose and the RT implant. This technique is preferred for forming a relatively thin BOX region of about 1200 Ã□or less, using a relatively low oxygen dose of about $2x10^{17}$ ions/cm^2 or less. Because of the simplicity of the process, this is also one of the most cost-effective ways of making high quality BOX layers.

[0028] The first step in the process is the base dose implant 310, as shown in Figure 3, which is performed at a first energy level E_{b1}. The next processing step is the RT implant 320, performed at a second energy level E_{rt1}. E_{rt1} is preferably lower than E_{b1} in value. Performing the RT implant at a lower energy than the base dose implant results in a tighter distribution of oxide precipitates during the high temperature annealing

process 330 which follows. This, in turn, reduces the amount of silicon (Si) inclusions in the BOX during the internal oxidation step. Thereafter, post-processing etch, cleaning and testing procedures may be selectively conducted to ensure device performance, as shown at 340.

[0029] Figure 6 graphically illustrates Si island inclusion density in the BOX from conventional SIMOX as shown at the curve 600 and the improved SIMOX as per one embodiment of the present invention, as shown at curve 610. The reduction of the inclusion size and density in the improved SIMOX clearly contributes to the improved breakdown voltage of the material.

[0030] It is important to determine the differential between the base dose energy and the RT implant energy. If the differential is excessive, it can degrade the surface smoothness of the SOI layer, as shown in Figure 7. A preferred differential between base and RT implants is calculated to be about 10% or less of the base dose energy.

[0031] An illustrative example can now be used to further demonstrate the improved SIMOX process as provided by the present invention. In this example, a process sequence is used to produce an SOI substrate with a nominal Si thickness of 700 Ã□and a high voltage BOX thickness of about 1350 Ã□Starting with a bulk silicon substrate, a base dose oxygen implant is first performed. In this illustrative example, the dosage for this implant is at 2.5 x 10^{17}ions/cm^2. The base dose implant is conducted at an energy E_{b1} of 180 KeV. The wafer temperature is kept at 365Â°C.

[0032] A room temperature implant is then conducted. The dosage for the RT implant in the illustrative example is at 2.0 x 10^{15} ions/cm^2. The RT implant is conducted at an energy level E_{rt1} which is at 165 KeV. E_{rt1} is therefore lower than E_{b1} in this example by about 8 percent An anneal is then conducted at a temperature of 1320 degrees Celsius for a total of 15 hours with an Argon ambient having between about 4% and 45% oxygen. After the anneal, a BOX layer having increased breakdown voltage results. A graph of the BOX breakdown voltage for the improved BOX process is shown in Figure 8.

[0033] The base dose implant can be performed either as a single step or in multiple steps. The total dose, however, for all base dose implants preferably ranges between 1x10^{16} and 4x10^{17}ions/cm^2 at a preferred energy between about 40 KeV and 240 KeV. The RT dose implant also can be done in single or in multiple steps to a total dose ranging between 5x10^{14} to 1x10^{16}ions/cm^2, at an energy between 10% and 20% lower than the base dose implant. Alternative embodiments of the present invention having multiple base implants and RT dose implants are described relative to Figures 4 and 5 below.

[0034] In Figure 4, an alternative embodiment of the present invention is provided having multiple base dose implants. In this embodiment, only a single RT implantation process is shown. Multiple base dose implants are preferred in situations where a high quality BOX layer is desired. The thickness of the BOX layer in such situations is usually greater than 1200 ÃIt is also preferable to use an oxygen dose of 2x10^{17}

ions/cm^2 or higher to achieve better results.

[0035] The first base dose implant, as shown at 410, is performed at a first energy level E_{b1}'. A second base dose implant 420 is then performed at a different energy level E_{b2}'. It is preferable that the second energy level E_{b2}' be lower than the first energy level E_{b1}'. In a preferred embodiment, the value of E_{b2}' is 5 to 10 percent lower than the value of E_{b1}'. It should be noted that although, for illustrative purposes, only two base implantation processes are discussed in the illustrative example of Figure 4, it is possible to utilize many base dose implants, each with different energy levels E_{b1}' to E_{bn}', where n is the total number of implantation steps for base dose implants. Preferably, each subsequent implant step is conducted at a lower energy level than the step before it.

[0036] It should be noted that incorporating wafer cleaning techniques between implant steps results in reduced density of BOX shorts and blocked implant defects, in addition to improved breakdown voltage. Furthermore, the BOX layer is usually formed at the location defined by the last (or the second, in case of Figure 4) base dose implant and the subsequent RT implant steps.

[0037] The first (or early) base dose implant(s) at higher energy provides additional oxygen to the BOX forming at shallower region during the high temperature anneal, which enhance the ITOX process of the BOX. This improves the breakdown voltage of the BOX even further.

[0038] After the base dose implanting is completed, a single RT dose implant process 430 is conducted at an energy level of E_{rt1}' which is a different energy level than either E_{b1}' or E_{b2}' in the example shown in Figure 4. It is preferable for the value of E_{rt}1' to be lower than all the base dose energy levels. The preferred energy differential between the second base dose implant, and the RT implant is about 10% or less of the second base implant energy E_{b2}'. The preferred differential between the two base implant energies is about 20% or less of the first base implant energy E_{b1}'. After the RT implant, a high temperature anneal 440 is performed, which is preferably followed by post-processing etching, cleaning and testing, as shown at 450.

[0039] A third embodiment is shown in Figure 5. In Figure 5, multiple RT implants are performed, but only with a single base dose implant. This embodiment is preferable in situations where the formation of a BOX layer having a thickness of 1600 ÃCbr greater is desired, needing an improved breakdown voltage. This is because the additional damage done by the RT implant will enhance the amount of internal oxidation (ITOX) during high temperature annealing and therefore provide a higher quality oxide in the BOX. Moving the location of the RT implant with respect to the base implant can also lead to a thicker BOX as well, which may be even more desirable to prevent post-SIMOX damage to the BOX.

[0040] As shown in Figure 5, the base dose implant step 510 is conducted at an energy level E_{b1}". The base dose implant step is followed by a first

RT implant step 520 which is conducted at a different energy E_{rt1}". E_{rt1}" is preferably lower than the base dose implant energy. In an embodiment, the difference between the base dose implant energy and the first RT implant energy is 5 to 10 percent. A second RT implant step 530 is then conducted at an energy level E_{rt2}" which is different from both the base dose energy E_{b1}" and the second RT energy E_{rt1}". In a preferred embodiment, E_{rt2}" is lower than E_{rt1}", preferably by 5 to 10 percent.

[0041] Again, as in the case of the previous embodiment, even though in this illustrative example only two RT dose implant processes are utilized, it is possible to use many RT implants, each having a different energy level E_{rt1}" to E_{rtm}", where "m" represents the number of RT processes. In a preferred embodiment, each subsequent energy level has a value that is lower than the base dose implant energy E_{b1}", as well as the RT energy level preceding it. A high temperature annealing process is then conducted at 540, followed by a selective etching/cleaning/testing process 550 to test for performance and provide a desired surface.

[0042] It should be noted that although the embodiments of Figure 4 and 5 each provide implantations involving multiple base dose implants and a single RT dose implant, or alternatively, a single base dose implant and multiple RT dose implants, it is possible to combine the two situations as to provide multiple base dose implants with multiple RT dose implants, each implant preferably having a distinct energy level that is preferably lower than the energy level of the preceding implant, as

discussed above.

[0043] In either case, the embodiments of the present invention, through various combinations of multiple base dose implants at varying energies, followed by precise offset in energies for the RT implants above and or below the BOX, can lead to a BOX having an improved breakdown voltage, with more processing capability, which is more charging resistant than conventional SIMOX processes. This same concept is reflected in Figure 9 below.

[0044] Figure 9 is a graph illustrating a relationship between the BOX breakdown voltage versus BOX thickness for various processes. It should be noted that while other SIMOX processes outside the scope this application may provide ways to produce an initial improvement in the BOX breakdown voltage, it is the strength of the BOX after it is thinned during subsequent processing that is most important. Furthermore, the graph of Figure 9 shows differing thinned BOX breakdown results (processes A, B and C), which indicates that different slopes exist between the initial BOX breakdown voltage and thinned BOX breakdown voltage. Consequently, it does not follow that any SIMOX process, when measured at initial full thickness before other processing, can predict results for a BOX layer thinned by subsequent processing that are acceptable except for the improved specific combinations that are provided by the present invention.

[0045] While the invention has been described in accordance with certain preferred embodiments thereof, those skilled in the art will understand

the many modifications and enhancements which can be made thereto without departing from the true scope and spirit of the invention, which is limited only by the claims appended below.